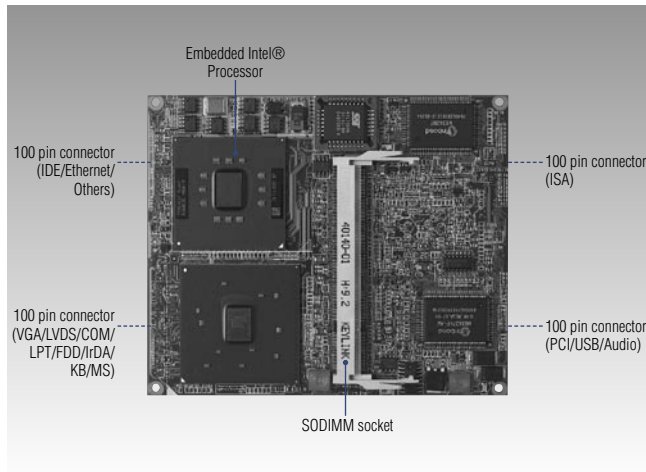


# SOM-4486 Series

Intel® Celeron® M SOM-ETX  
Module with CPU, VGA/LVDS,  
Audio & LAN



## Specifications

- **CPU** Embedded Intel Celeron M processor w/64 KB primary cache memory
  - **System Memory** 1 x 200 pin SODIMM sockets, support Double Data Rate (DDR) 128 MB to 1 GB, accept 128/256/512/1024 MB DDR200/266/333 DRAM
  - **System Chipset** Intel 852GM GMCH/ICH4 Chipset 400 MHz PSB
  - **BIOS** AWARD 4 Mbit Flash BIOS
  - **WatchDog Timer** 255 levels timer interval, from 1 to 255 sec or min setup by software, jumperless selection, generates system reset
  - **Expansion Interface** Support PCI & ISA interface
- I/O**
- **MIO** 2 x EIDE (UDMA 66), 1 x LPT/FDD (shared), 1 x K/B, 1 x Mouse, 2 x RS-232,
  - **IrDA** 115 Kbps, IrDA 1.1 compliant.
  - **USB** 4 USB 2.0 compliant ports
- Ethernet**
- **Chipset** Intel 82562EZ
  - **Ethernet Interface** IEEE 802.3u 100Base-T compatible

## Features

- Embedded Intel® Celeron® M processor
- Supports DDR Memory
- With Vcore 2 phase design for more stable system
- 4 x USB 2.0 ports
- Supports up to dual channel LVDS panels

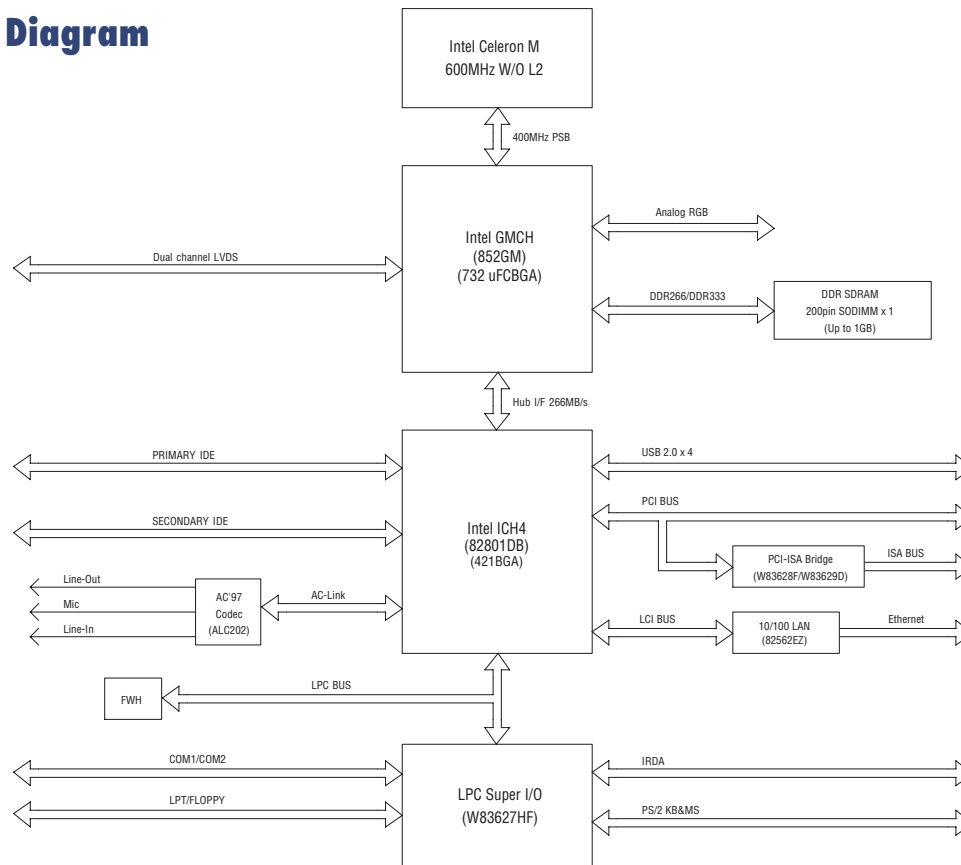
## Display

- **Chipset** Intel 852GM
- **Memory Size** Optimized shared memory architecture, supports 1 MB/8 MB frame buffer using system memory
- **Resolution**
  - \* CRT Display mode Pixel resolution up to 1600 x 1200 at 85 Hz and 2048 x 1536 at 75 Hz
  - \* LCD Display mode Dual channel LVDS panel supports up to UXGA panel resolution with frequency range from 25 MHz to 112 MHz

## Mechanical and Environmental

- **Dimensions (L x W)** 95 x 114 mm (3.74" x 4.5")
- **Power Supply Voltage** +5 V power only
- **Power Requirement** Max: +5 V @ 2.2 A, Typical (256 MB DDR 333): +5 V @ 2.6 A
- **Operating Temperature** 0 ~ 60° C (32 ~ 140° F)
- **Operating Humidity** 0% ~ 90% relative humidity, non-condensing

## Board Diagram



## Ordering information

### Standard

- **SOM-4486FL-M0A2E** Intel Celeron M ULV 600 MHz SOM-4486
- **SOM-4486FL-Q0A2E** Intel Celeron M ULV 800 MHz SOM-4486
- **SOM-DB4400-00A2** SOM-ETX Development Board Rev. A2